

Error Type	Error Code	Additional Digits	Error Name	Transmitter	Receiver	Control Unit	Description	
Setup Errors	11	-	DIP Switch Error	●	●		DIP switch setting does not correspond with the timing of the overflow signal.	
	12	-	CPU Select Error		●	●	The MASTER/SLAVE pin strapping is not as expected by software	
	13	-	CPU Oscillator Error	●	●	●	CPU couldn't start ext. oscillator, or ext. oscillator failed	
	18	1	Jumper Disagree Error		●	●	●	The processors do not agree on the state of the jumper input.
		2	Jumper No Drive		●	●	●	Failure of the jumper test circuit – drive bit stuck inactive.
3		Jumper Changed Error		●	●	●	The jumper inputs have changed state since power-up.	
	4	Jumper Hi No Drive		●	●	●	Failure of jumper test circuit – reading inputs when not enabled.	
Software Errors	21	1	Task call count mismatch	●	●	●	Safety-critical task call count not as expected	
		2	Self-monitor progress mismatch	●	●	●	Self-test progress counter mismatch between CPUs	
	22	-	Stack Error	●	●	●	Software stack was overwritten or overflowed	
	23	-	Safety Variable Error	●	●	●	Redundantly-stored software variable was corrupt	
	24	-	Scheduler Error	●	●	●	CPU unable to complete all scheduled tasks within one system tick	
	25	-	Invalid Interrupt Error	●	●	●	An unused interrupt was triggered	
	26	-	System Tick Interrupt Error	●	●	●	System tick interrupt was late	
29	-	Internal Error	●	●	●	Impossible internal condition, e.g., array index out-of-bounds.		
Hardware Errors	31	-	CPU Flash Error	●	●	●	Flash memory CRC does not match stored CRC.	
		-	CPU RAM Error	●	●	●	CPU RAM failed address or data test.	
	33	-	CPU ADC Error	●	●	●	CPU ADC failed or incomplete	
		1	CPU ADC voltage monitor error	●	●	●	Optics/logic supply out of range	
		2	CPU ADC voltage monitor error	●	●	●	reference voltage out of range	
		3	CPU ADC voltage monitor error	●	●	●	ground voltage out of range	
		4	CPU ADC voltage monitor error	●	●	●	24V system supply voltage out of range	
	34	1 + instr# ②	CPU Op-code Error	●	●	●	CPU Op-code test failed	
		2	CPU Register Error	●	●	●	CPU register test failed	
	35	1	Watchdog Clear Error	●			The processor was not able to clear the hardware watchdog circuit.	
		2	Watchdog No Trip Error	●			The processor was not able to force a trip of the hardware watchdog.	
		3	Watchdog Timed Out Error	●			The processor detected a TIMEOUT of the hardware watchdog.	
	36	-	Scan Disagree Error		●		The processors disagreed on the result of a bar scan	
	37	1	OSSD Feedback Not ON Error	●	●		OSSD feedback did not properly report the "ON" state.	
		2	OSSD Feedback Not OFF Error	●	●		OSSD feedback did not properly report the "OFF" state.	
	38	1	OSSD Test Error (master enable)	●	●		Master CPU output enable test failed	
		2	OSSD Test Error (slave enable)	●	●		Slave CPU output enable test failed	
		3	OSSD Test Error (master disable)	●	●		Master CPU output disable test failed	
		4	OSSD Test Error (slave disable)	●	●		Slave CPU output disable test failed	
		5	OSSD Test Error (master 3v)	●	●		Master CPU 3v-too-high test failed	
6		OSSD Test Error (slave 3v)	●	●		Slave CPU 3v-too-low test failed		
39	1	MPCE Invalid Configuration	●			MPCE monitoring enabled with control unit connected		
	2	MPCE Not Tracking		●	●	The state of the MPCE input does not agree with the state of the OSSDs – MPCE mode is enabled.		
		MPCE Not Static		●	●	The processors detect the MPCE input line is not static when the MPCE function has been disabled.		
	4	MPCE Hi Bits No Drive	●	●		Failure of MPCE test circuit – reading inputs when they are not enabled.		
	5	MPCE CPUs Disagree	●	●		The processors do not agree on the state of the MPCE input line.		
6	MPCE No Drive	●	●		Failure of MPCE test circuit – drive bit stuck inactive.			
Inter-Processor Communication Errors	41	-	Timeout		●	●	The reporting processor experienced a TIMEOUT waiting for communication with the companion processor.	
	42	-	Incorrect packet sequence	●	●		CPUs disagreed on packet sequence number	
	43	-	Invalid packet length	●	●		The reporting processor detected an improper packet length in the communication with the companion processor.	
	44	-	Bad CRC	●	●		The reporting processor detected a CRC error on the last packet during communication with the companion processor.	
	45	-	Timer sync failure		●	●	Attempt to synchronize the processor clocks failed – too far out.	
	46	-	Bad packet source		●	●	Unknown/incorrect packet source field	
Serial Errors	51	-	Serial Timeout Error		●	●	Serial data timeout, after some characters were received	
	52	-	Serial No Data Error		●	●	Serial data timeout, no characters received	
	53	-	Serial Receive Error		●	●	UART error flag detected.	
	54	-	Serial Sequence Error		●	●	Serial packet sequence number mismatch.	
	55	-	Serial Length Error		●	●	Serial packet length out-of-bounds.	
	56	-	Serial Bad CRC Error		●	●	Received packet CRC does not match packet contents.	
	57	-	Serial Retries Error		●	●	Too many (5+) retries to send a packet.	
	58	-	Serial Bad Response Error		●	●	Illegal/invalid response to serial packet received	
	59	-	Serial packet mismatch		●	●	CPUs built different data packets for transmission to other unit	
Light Bar Errors	61	CH # ①	Channel Loop-back HI (0 Channels Enabled)	●	●		Channel loop-back active (HI) with 0 channels enabled – should be LOW.	
	62	CH # ①	Channel Loop-back LOW (1 Channel Enabled)	●	●		Channel loop-back inactive (LOW) with 1 channel enabled – should be HI.	
	63	CH # ①	Channel Loop-back HI (2 Channels Enabled)	●	●		The Channel Loop-back signal is active (HI) with 2 channels enabled (scan logic test) – should be LOW.	
	64	CH # ①	Channel Overflow Early	●	●		OVFL active before end of bar scan	
	65	CH # ①	Channel Overflow Late	●	●		OVFL still inactive at end of bar scan	
	661	CH # ①	Channel Clock Not Detected	●			RX_MON didn't detect a channel clock signal when one was expected	
	662	CH # ①	Extra Channel Clock Detected	●			RX_MON detected multiple channel clock signals when one was expected	
	67	-	Channel Reset Error		●		RX_MON saw channel reset in wrong state	
69	-	Sync-enable mismatch		●		RX_MON didn't detect active SYNC_EN signal when expected		
Control Unit Errors	73	1	Key Switch No Drive		●		Failure of the key switch test circuit – drive bit stuck inactive.	
		2	Key Switch Hi No Drive		●		Failure of the key switch test circuit – reading inputs when not enabled.	
		3	Key Switch Disagree Error		●		The processors disagree about the state of the key switch.	
	75	-	Couldn't drive Set/Reset switch		●		CU_MON didn't detect an active set/reset switch drive circuit when expected	
	76	-	Set/Reset Switch Disagree Error		●		The processors did not agree on the state of the Set/Reset switch.	
	77	-	Interlock Out Error		●		The processor detected a problem with the operation of the INTERLOCK status output to the Receiver bar.	
	78	1	OSSD Interrupt Too Late		●		OSSD shutoff interrupt not detected	
	78	2	OSSD Interrupt Timeout		●		Periodic OSSD test related interrupt not detected	
79	-	Programming Mismatch		●		CU's CPUs don't agree on setup options (blinking modes)		

① Blinks out the faulty channel number after the error code, e.g., "6432" for "channel overflow early - on channel 32".

② Blinks out the instruction test table index after the error code, refer to source to determine instruction

Note: Digits containing a zero have a blink code of '10'. A two-digit blink code of '70' is represented by 7 blinks followed by 10 blinks.